ABSTRACT OF THE DISCLOSURE

A circuit and method for multi-bit processing of a gray scale image in a printer. In the multi-bit processing circuit, a divider divides the gray component value of each pixel in a multi-bit image by the resolution of the printer and outputs the quotient. A remainder calculator outputs the remainder of the division for the input of the gray component value. A half-tone table stores half tone values corresponding to thresholds for pixels. A comparator compares the remainder with a corresponding threshold half tone value received from the half-tone table and outputs a binary bit according to the comparison result. A position controller controls the half-tone table to repeatedly output the threshold half tone value of each pixel. An adder adds the quotient received from the divider to the gray component of the binary processed output of the comparator, pixel by pixel and outputting a multi-bit dithered image. A pulse width modulator modulates the multi-bit dithered image received from the adder to different pulse widths according to the gray components of the pixels of the multi-bit dithered image and controls the modulated image to be printed in dots of different sizes.